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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DOAN, NGHIA M	

ART UNIT	PAPER NUMBER
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/552,759	URIU ET AL.	
	Examiner	Art Unit	
	NGHIA M. DOAN	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is response to the Applicant Amendment filed on 11/06/2008. Claims 1-11 remain pending.

Claims 1 and 11 have been amended.

Claims 12-18 have been canceled.

The amended specification is accepted.

The amended abstract is accepted.

Claim rejection under 35 U.S.C 112 second is withdrawn.

Response to Arguments

2. Applicant's arguments with respect to claims 1 and 11 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-11are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al., (Full-Wave Segmentation Analysis of Arbitrarily Shape Planar Circuit, 1997, IEEE, page 1-9).

5. With respect to claims 1 and 11, Liu teaches a method and apparatus for analyzing an electromagnetic field (EM) of a circuit board based on shapes of conductor

patterns and signal analysis conditions (the abstract, see fig. 1a-1b descriptions) including steps of:

setting up initial shapes of conductor patterns in each layer of a multilayer circuit board (a plane printed/microwave circuit of arbitrary shape is printed on a system of stratified substrate) (see fig. 1a) ;

setting up initial ports for input or output of an external signal in each conductor pattern (two external ports are connected to blocks A and B) (see fig. 1b);

dividing two-dimensionally the multilayer circuit board into a plurality of areas such as a first layer of the multilayer circuit board is divided into a plurality of areas using dividing lines (dividing the printed circuit into four smaller segments denoted as blocks A, B, C, D and dividing lines (dash lines) on surface of block shown as fig. 1a and also dividing lines (dash lines) shown as fig. 8) (see fig. 1a);

setting up additive ports on edges of the conductor pattern which has been created by area-division (input or output ports are placed across the interconnecting lines between the adjacent blocks) (see fig. 1b);

setting up individual analysis conditions (magnetic current sources, as incident waves and reflected waves, thickness, width, height of conductors, etc.) for the initial ports and the additive ports, respectively (pages 3-4, section A, Equivalent Source of a Segmented Circuit and section B, GSM Space-Domain Integral Equation, also see fig. 2 and fig. 3);

performing an electromagnetic analysis of the multilayer circuit board by the divided area, based on the analysis conditions (the EM field in the individual segments

can be uniquely determined by knowledge of the tangential electric (magnetic) fields over the corresponding reference plane) (see page 2, col. 2, section II, Model and GSM Space-Domain Integral equation method); and

integrating results of the electromagnetic analysis over each of the divided areas, thereby obtaining results of the electromagnetic analysis over the whole circuit board (combination of these GSM's yield an overall network characterization of composite circuit) (the abstract, section I, introduction, and section II, Model and GSM Space-Domain Integral equation method).

Liu does not implicitly teach further layers of the multilayer circuit board are divided correspondingly using the same dividing lines.

But Liu teaches a reference planes (the same dividing lines to other layers) are placed across the interconnecting lines between adjacent blocks to define the input or output port for the respective segments (see fig. 1b) and Liu also teaches to place two fictitious electrical wall at the reference planes RP1 and RP2 (see sig. 2 and also see fig. 3 as three dimensional of cross section of divided blocks).

Therefore, it would have been obvious one of ordinary skill in the art would appreciated the segmentation method for analyzing a complex and large microwave planar circuit which is divided into several segments/blocks in three dimensional (3D) using the reference planes are placed across the interconnecting lines between adjacent blocks (as equivalent dividing lines to further layer) that benefits of less memory usage, reducing total CPU time process, and only one or few segment in

microware circuit need modification when tuning or optimizing the circuit without resorting to change all the segment network (section 1 introduction).

6. With respect to claim 2, Liu teaches the method for analyzing an electromagnetic field of a circuit board according to Claim 1, wherein in the step of dividing the multilayer circuit board into a plurality of areas, the multilayer circuit board is divided two-dimensionally into a plurality of areas using dividing lines including a plurality of straight lines parallel to each other (see fig. 1a, and also see fig. 8 as line L1, L2, and L4).

7. With respect to claim 3, Lui teaches method for analyzing an electromagnetic field of a circuit board as dividing two dimensionally the multilayer circuit board into a plurality of areas using dividing lines including a plurality of straight lines (see fig. 1a)

Lui doe not implicitly teach the dividing straight lines are perpendicular to each other.

It would have been obvious to one of ordinary skill in the art that the dividing straight lines perpendicular to each other, which is created a 90 degree angle as a special case of an arbitrary angle that reduces a complexity for performing EM analysis in dividing two dimensional (planar plane) and easier to set up an electric and magnetic field tangential to the reference planes.

8. With respect to claim 4, Lui teaches the method for analyzing an electromagnetic field of a circuit board according to Claim 1, wherein in the step of dividing the multilayer circuit board into a plurality of areas (see fig. 1a), the multilayer circuit board is divided two-dimensionally into a plurality of areas using dividing lines including a polygonal line

or a curved line (straight line is specially of polygonal or curved line) (see fig. 1a and fig. 8).

9. With respect to claim 5, Lui teaches the method for analyzing an electromagnetic field of a circuit board according to Claim 1, wherein in the step of dividing the multilayer circuit board into a plurality of areas (see fig. 1a), shapes of the dividing lines are designated using a pointing device while representing a plan view of the multilayer circuit board on a display screen (see fig. 1a, fig. 3 and fig. 8).

10. With respect to claim 6, Lui teaches the method for analyzing an electromagnetic field of a circuit board according to Claim 1, including a step of calculating the number of the edges of the conductor pattern created by area-division (see Section A, Equivalent Source of a Segmented Circuit, also see fig. 1b).

11. With respect to claim 7, Lui teaches the method for analyzing an electromagnetic field of a circuit board according to Claim 6, wherein in the step of setting up additive ports, the ports are added, the number of which corresponds to the calculated number of the edges (expansion number of modes [Mv] as physical ports) (see Section A, Equivalent Source of a Segmented Circuit, also see fig. 1b).

12. With respect to claim 8, Liu teachesthe method for analyzing an electromagnetic field of a circuit board according to Claim 1, wherein in the step of setting up additive ports, the ports are added in the center of the edge (see fig. 1b).

13. With respect to claim 9, Liu teaches the method for analyzing an electromagnetic field of a circuit board according to Claim 1, wherein, when a position of one port located on the edge of a conductor pattern residing in one layer (fig. 2 and 3b, [RP1])

coincides with a position of another port located on the edge of another conductor pattern residing in another layer (fig. 2 and 3b, [RP1]), one of the ports is displaced to be represented on a display screen (see fig. 2 and fig. 3a-3b and also see fig. 8).

14. With respect to claim 10, Liu teaches the method for analyzing an electromagnetic field of a circuit board according to Claim 1, including steps of: changing the shape (arbitrary shapes) of the conductor pattern residing in a particular divided area, to perform again the electromagnetic analysis over the particular divided area (a plane printed/microwave circuit of arbitrary shape is printed on a system of stratified substrate) (see fig. 1a); and integrating a result of the electromagnetic analysis over the divided area with the result of the electromagnetic analysis over the another divided area, thereby obtaining results of the electromagnetic analysis over the whole circuit board (combination of these GSM's yield an overall network characterization of composite circuit) (the abstract, section I, introduction, and section II, Model and GSM Space-Domain Integral equation method).

Response to Arguments

15. Applicant's arguments filed 11/06/2008 have been fully considered but they are not persuasive. The claim rejection is sustained as the following reason:

35 USC 102 and/or 103

16. Applicant argues "Liu, Figs. 1a and b fail to disclose or suggest details of port settings **during** area-division. Liu also fails to disclose or suggest how to set up any ports for electrodes of all elements (including dielectrics required for area-division).

17. Examiner respectfully disagrees with Applicant as the following:

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., detail of port settings during area-division and how to set up any ports for ports for electrodes of all elements (including dielectrics required for area-division) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Moreover, Lui teaches or suggests four additional reference planes (the same dividing lines to other layers) are placed across the interconnecting lines between adjacent blocks to define the input or output port for the respective segments that is at least suggest detail of how to set up ports for area-division (see fig. 1b, the equivalent segmented multiport GSM model; and section **II**. Model and GSM space domain integral-equation method).

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. PTO-892.

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NGHIA M. DOAN whose telephone number is (571)272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nghia M. Doan
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